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Holistic Approaches for Integrity of **ICT-Systems**

HINT aims to develop a set of solutions for the implementation of a framework for a systemos integrity checking based on Trusted Computing technologies. Moreover, the capabilities of the developed technologies will be demonstrated on reallife applications. It is planned to prepare the adoption of the proposed technologies by future Common Criteria evaluation schemes.

Main Project Information

Message from the Coordinator

The first half of the 2nd period of the HINT project has almost passed. One deliverable - **Q2.1 Report on novel** cell and architecture concepts based on technology dependent research+- has been submitted and a lot of effort is currently being put in the preparation of a number of upcoming deliverables.



Partners at Technical Meeting in Dresden, March 2014

ages - such as the WP3 meeting in Gardanne and the WP2 meeting in Villach - have taken place. Several partners also met for technical discussions in Dresden and Paris in order to ensure smooth progress and the achievement of all planned objectives. The past two quarters were characterised by the FPGA implementation of the PUF emulator as well as first candidates of ECC in hardware. Moreover, technologies enabling the detection of Hardware Trojans and functional clones have been developed and evaluated. Also, preparation work for the integration of

A couple of telcos and meetings dedicated to specific work pack-

Participation in Conferences, Workshops and Events

- Cartes 2013, 19th 21st November 2013, Paris/FRANCE
- TRUDEVICE, 12th 13th December 2013, Lisbon/PORTUGAL
- HiPEAC 2014, 20th 24th January, Vienna/AUSTRIA
- RSA Conference, 24th 28th February 2014, San Francisco/USA
- EU Cybersecurity Strategy, 28th February 2014, Brussels/BELGIUM
- DATE 2014, 24th 28th March 2014, Dresden/GERMANY
- Smart Systems Integration, 26th 27th March 2014, Vienna/AUSTRIA
- Security Solutions Tech Days, 3rd 4th April 2014, Elancourt/FRANCE
- Trust in the Digital World Conference, 7th 8th April 2014, Vienna/AUSTRIA
- Cyber Security & Privacy Forum, 21st 22nd May 2014, Athens/GREECE

Key Data:

Start Date: End Date: Duration:	1 October 2012	
	30 September 2 36 months	
		Project Reference:
Project Costs:	" 5.103.893	
Project Funding:	" 3.350.000	

ber 2015

Consortium: Project Coordinator: Technical Leader:

Project Website:

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The HINT project has received funding from the Euro-UnionIs Seventh Framework Programme pean (FP7/2007-2013) under grant agreement number ICT-317930.

a HW anchor as peripheral in ID-card architecture has been performed and alternative concepts are being evalu-

ated.

From an administrative point of view the Forms C have been processed and communicated to the Project Officer and the payment of the second tranche has been transferred.



June 2014



TRUDEVICE

Upcoming Events

Training School on Trustworthy Manufacturing and Utilization of Secure Devices 14th - 18th July, Lisbon/PORTUGAL (Talk of HINT project partner Cassidian Cybersecurity SAS)

Chip-to-Cloud Security Forum

22nd - 25th September, Marseille/FRANCE (Presentation about % Holistic Integrity Checking of ID Cards+by Morpho)

HINT on the web - www.hint-project.eu

All **HINT** related news, like upcoming meetings and conferences, as well as HINT related scientific publications and other dissemination material can be found on our **project website**. In addition to that, all public deliverables will be uploaded and made accessible on our project website after official approval by the European Commission.

Furthermore, Cassidian Cybersecurity SAS has published a **blog** entry, being the 5th most read article, describing and promoting the HINT project.

Outlook for the second half of the HINT Project Year 2

Due to a tight schedule the next months will be busy ones. Several deliverables and one major milestone will arise until the end of year 2, which is characterised by holistic integrity checking and the development of functional prototypes. Integrity checking addresses the detection of Hardware Trojans, the detection of functional clones and the detection of counter-feited components. A further focus will be put on the implementation of cell arrays and optimized post-processing of novel hardware integrity anchors. Moreover, the project partners will investigate on already known and novel attacks as well as on countermeasures in order to protect against such attacks. A wide range of tests, including physical attacks (e.g. allowing modification of the device or access to internal signals), Side Channel Analysis (time, consumption, electromagnetic) and fault injections (glitches, laser, EM) will be performed under various environmental conditions. Robust and secure protocols to prevent impersonation attacks will be defined and implemented In a further step they will be integrated in the respective use cases - Professional Mobile Radio Equipment and Non-Clonable ID-Cards. Another important aspect that will characterise the upcoming months is the security evaluation of the proposed technologies and the prototype testing. With

the planned accomplishment of MS3 in M24, the development phase for HW integrity checking will be concluded and the corresponding demonstrator will be built and functional.



FPGA Prototype Board

Upcoming Deliverables & Milestone

- D2.2 FPGA-prototype including advanced post-processing methods and techniques
 - D3.1 Report on protocol choice and implementation
 - **D3.2** Report on detection methodology and performances
 - D3.3 Prototype (FPGA based) of the hardware integrity checking primitives
 - **D4.1** Report on the integration of a hardware security anchor
 - **D6.3** Report on dissemination, exploitation and standardisation
 - D6.6 Second annual report according to EC regulations of the model contract
- MS3 End of development Phase

HINT Project Coordination Team

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